2815

PATENT
Customer No. 22,852
Attorney Docket No. 04329.2270-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Shinsuke SAKAMOTO et al.

Application No.: 10/081,109

Filed: February 25, 2002

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND WIRING ARRANGING METHOD THEREOF

Group Art Unit: 2815

Examiner: Eugene Lee

#8 Amdt 8/26/03



Commissioner for Patents
Washington, DC 20231

Sir:

**AMENDMENT**

In reply to the Office Action dated November 18, 2002, the period for reply extending to February 19, 2003 (the federal government being closed on February 18, 2003 due to inclement weather), please amend the application as follows:

**IN THE CLAIMS:**

Please cancel claims 4, 5, 9, and 11-14 without prejudice or disclaimer of the subject matter thereof, amend claims 1 and 10, and add new claims 15-20, as follows:

1. (Amended Three Times) A semiconductor integrated circuit device, comprising:

first and second I/O slots arranged on the same wiring level in parallel along a peripheral portion of a chip within an inner region of the chip;

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